THRESHOLD VOLTAGE MODELING OF RECESSED SOURCE/DRAIN SOI MOSFET WITH VERTICAL GAUSSIAN DOPING PROFILE

A dissertation submitted in partial fulfilment of the requirements for the degree of

MASTER OF TECHNOLOGY
IN
VLSI DESIGN AND EMBEDDED SYSTEM

by

MUKESH KUMAR KUSHWAHA
ROLL NO: 213EC2202

to

Department of Electronics and Communication Engineering
National Institute of Technology
Rourkela, Orissa, India
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DEPARTMENT OF ELECTRONICS AND
COMMUNICATION ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY, ROURKELA
ODISHA, INDIA-769008

CERTIFICATE

This is to certify that the thesis report entitled "**Threshold Voltage Modeling of recessed source/drain SOI MOSFETs with vertical Gaussian doping profile**" submitted by **MUKESH KUMAR KUSHWAHA**, bearing **Roll No. 213EC2202** in partial fulfilment of the requirements for the award of **Master of Technology in Electronics and Communication Engineering** with specialization in "**VLSI Design and Embedded System**" during session 2013-2015 at National Institute of Technology, Rourkela is an authentic work carried out by him under my supervision and guidance.

To the best of my knowledge, the matter personified in the thesis has not been submitted to any other university/institute for the award of any Degree.

Place: Rourkela
Date: 20th May, 2015

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Dedicated to

My beloved family

ACKNOWLEDGEMENT

I would like to thank my project supervisor **Prof. (Dr.) P.K.Tiwari** whose guidance and support helped me at every step of the research done as well as thesis eriting. He encouraged me all the time and kept me motivated and inspired. He helped me to overcome all hurdles in my work.

I am very grateful to Prof. (Dr.) K.K.Mahapatra, Prof.(Dr.) D.P Acharya, Prof.Ayas Kanta Swain, Prof. Shantanu Sarkar, Prof.(Dr.) Nurul Islam and all other faculties and staff of ECE Department, NIT Rourkela for their help and support. I am also very thankful to Mr. Gopi Krishna S, Mr. Visweswara Rao for discussing various topics and suggesting new ideas. I would also express my gratitude to my batch mates Mr. Mukesh Kumar, Mr. Santosh Padhy and Ms. Srikanaya for their support, guidance and suggestions. I am really thankful to all my classmates and other friends who had made my stay in NIT a pleasant experience.

Lastly I would like to express my highest gratitude for my family for their inspiration and encouragement.

MUKESH KUMAR KUSHWAHA

ABSTRACT

Recessed-source/drain silicon-on-insulator (Re-S/D SOI) MOSFETs are being researched in both academia and industry because of its high drain current drive capability. In a Re-S/D SOI MOSFET, source and drain regions are stretched into the buried oxide (BOX) in order to reduce the series resistance.

The electrical parameters are most important parts in defining the functionality of the device. First objective of the project work is to meet the electrical parameter specifications like threshold voltage, subthreshold swing, ON current and leakage current specified in ITRS 2011 and some other technical literature by adjusting of physical parameters like, silicon channel thickness, channel length and gate oxide thickness, that means it has to find out the physical parameters of the device for the standard values of electrical parameters. So, it has to maintain these device parameters for given specified values, the channel thickness, oxide thickness and gate length are adjusted accordingly.

Fully depleted Re-S/D SOI MOSFETs possess good short channel immunity and close to ideal subthreshold characteristics. A number of attempts have been done to model the subthreshold characteristics of Re-S/D SOI MOSFETs with undoped or uniformly doped channel for getting more physical insight. However, the actual doping profile after the ion implantation step differs from uniform profile and resembles much with the Gaussian profile. In addition, the Gaussian profile in turn gives two more parameters, projected range (R_P) and straggle (σ_p), which can control the device characteristics.

In this project work, an effort has been done to develop a novel model for the threshold voltage of Re-S/D SOI MOSFETs with vertical Gaussian doping profile in the channel. The two-dimensional Poisson's and Maxwell equation has been solved in the channel region of the

device considering the proper boundary conditions. The developed analytical model predicts the threshold voltage of the device for wide variations in the device parameters. MATLAB has been used for calculation of the analytical model results with variations in the device parameters. The model results are compared by the result obtained with ATLAS^{TM} device simulator to verify the accuracy of the model.

TABLE OF CONTENTS

LIST OF ACRONYMS

VLSI	Very Large Scale Integration
SOI	Silicon-on-insulator
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
Re-S/D SOI MOSFET	Recessed Source/Drain SOI MOSFET
BOX	Buried Oxide
ITRS	International Technology Roadmap for Semiconductor
CMOS	Complementary Metal Oxide Semiconductor
SCE	Short Channel Effect
HCE	Hot Carrier Effect
DIBL	Drain Induced Barrier Lowering

LIST OF SYMBOLS

t_{Si}	Silicon-body thickness
t_{GOX}	Gate-oxide thickness
t_{RSD}	Thickness of the source/drain extensions in the buried-oxide
t_{BOX}	Buried-oxide thickness
C_{GOX}	Gate-oxide capacitance
C_{Si}	Fully-depleted silicon-body capacitance
C_{BOX}	Buried-oxide capacitance
C_{RSD}	Recessed source/drain buried-oxide capacitance
k_{GOX}	Gate-oxide dielectric constant
k_{Si}	Silicon-body dielectric constant
d_{BOX}	Length of source/drain overlap over buried-oxide
k_{BOX}	Buried-oxide dielectric constant
K_{GOX}	Gate-oxide relative dielectric constant ($K_{GOX} = k_{GOX}/e_0$)
K_{BOX}	Buried-oxide relative dielectric constant ($K_{BOX} = k_{BOX}/e_0$)
L	Device channel length
$N_0(y)$	Silicon-body vertical Gaussian doping concentration
N_{Sub}	Substrate doping concentration
N_G	Gate doping concentration
N_{SD}	Source doping concentration
V_{FB1}	Front-gate flat-band voltage
V_{FB2}	Source/drain-back-gate flat-band voltage
V_{FB3}	Substrate-back-gate flat-band voltage

V_{th}	Threshold voltage
ψ_f	Front channel surface potential
ψ_b	Back channel surface potential
ϕ_{Si}	Channel (silicon-body) work-function
ϕ_M	Gate work-function
V_{bi}	Built-in potential
V_G	Gate voltage
V_{DS}	Drain–source voltage

LIST OF TABLE

LIST OF FIGURES

CHAPTER 1

INTRODUCTION

CHAPTER 1
INTRODUCTION

1.1 Semiconductors Materials

Semiconductor Physics is the branch of science which deals with behaviour of semiconductors. Semiconductors derive their name from the fact that they conduct the current better than insulators, but not as well as conductors. These materials have negative-temperature-coefficient (NTC) of resistance. The resistivity of the semiconductor materials are lies between $10^{-4} < \rho < 10^{8}$ Ω-m. The electrical properties of these materials can be varied with impurity content, temperature and optical excitation. Due to these changeability nature of the semiconductor materials, it is the usual choices for electronic devices for industrial and research work.

1.2 Semiconductor Devices

During past years, vacuum tubes, devised in 1905 by Ambrose Fleming were used as basic components in electronic devices. Although the first MOS transistor was invented by J.E. Lilienfeld in 1926 [1] (Fig 1.1) but the semiconductor devices became extremely popular after the invention of BJT in 1948 by Shockley, Bardeen and Brattain at Bell Telephone Laboratories, which replaced the vacuum tube in electronics field because of its small size, high efficiency, high stability, high durability and cheaper also in comparison to vacuum tubes. It was commercialized by Texas Instruments in 1954 by production of junction transistors for portable radios.

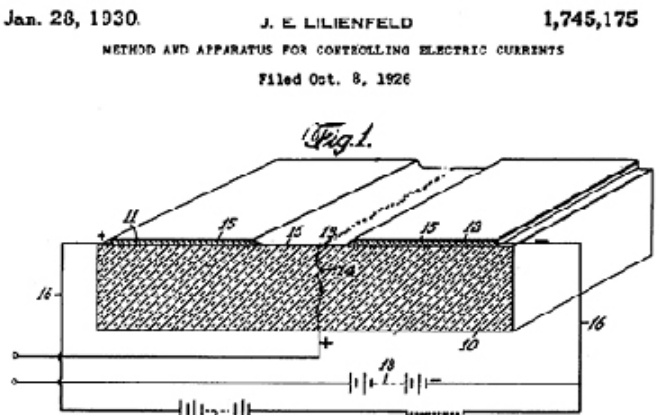

Fig 1.1 First MOS Transistor patented by J.E. Lilienfeld

The Field Effect Transistors (FET) were developed to improve the consistency of the device. The field effect transistor comes in several forms. In junction FET (JFET), the depletion width of reverse biased p-n junction varies with the applied gate voltage. The Metal Semiconductor FET (MESFET) was developed by junction by shottky barrier. Metal-insulator-semiconductor (MESFET) became an alternate device in the early 1960s, when two scientist, Kahng and Atalla developed demonstrated the techniques for growing the oxide layers. In the MESFETs, the metal gate electrode was separated from semiconductor by an insulator. MOSFET, stands for Metal Oxide Semiconductor Field Effect Transistor, is a special case of MESFET in which oxide layer is used as the insulator.

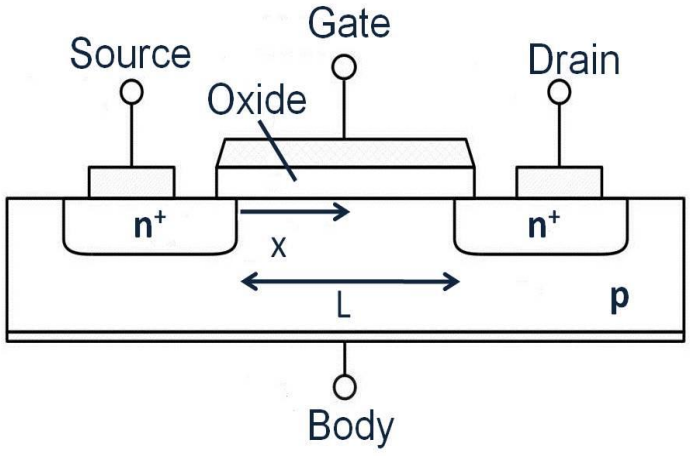

Fig. 1.2 The cross sectional view of n-channel MOSFET

MOSFETs are basically four terminal devices: Source, Drain, Gate and Substrate. The carriers transports from the source into drain across the channel region causes the conduction in the device. The silicon dioxide (SiO_2) is used as insulator which is sandwiched between polycrystalline gate and the channel region, region between source and drain. A simplified structure of MOSFET is shown in fig 1.2 (n-channel MOSFET) which doped with p-type semiconductor base.

1.3 Device Scaling

The historical trend for semiconductor devices has been constantly reduction of device dimensions which refers as device scaling. The scaling of device is starts with the insight of Lilienfeld of MOS Transistor which switch the vacuum tube with trivial size of semiconductor devices [1]. The idea of the integrated circuits (IC) was conceptualized by Jack Kilby in 1958 at Texas Instruments and the first IC was fabricated by Robert Noyce at Fairchild Corporation. "There is plenty of room at the bottom" is the prominent speech which was conveyed by Richard Feyman in 1959. In 1960s, Gordon Moore gave a statement that in every 18 moth, the number of transistors in the chip doubles which is called as Moore's law.

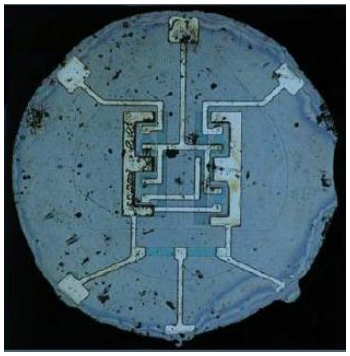

Fig 1.3 First IC fabrication at Fairchild Corporation

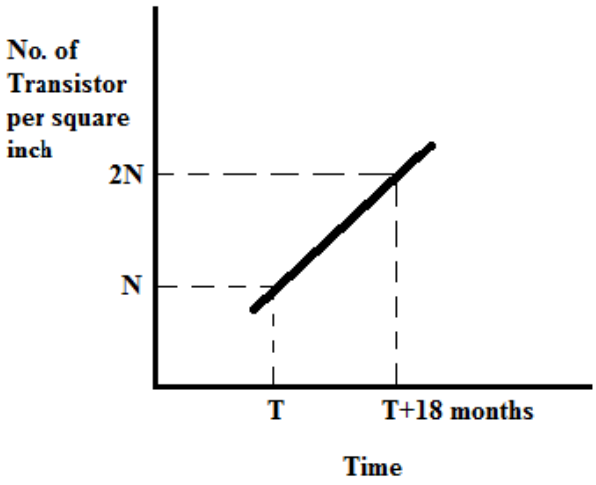

Fig 1.4 Chip density showing Moore's law

The miniaturization of the MOS ICs is the world's growing requirement which reduces the dynamic power consumption through lesser voltage and upsurge the packing density of the chip. It leads to cheaper, small sized and low power semiconductor devices through VLSI design. The scaling of MOS transistors improve the frequency response and current drive. However, it has been promising to incorporate of billions of transistors on a single chip by scaling of the device but there are many difficulties in fabrication of the device.

The reduction of the dimensions of transistors causes the change in the the operational characteristics of the MOSFETs. Some limitations restrict the extent the scaling. Scaling of the MOS transistors is apprehensive with efficient reduction of overall dimensions of the devices, while maintaining the geometric ratios defined in larger devices. The comparative scaling of the devices rise the density of the chip.

There are two scaling strategies:

1. Constant Field Scaling (Full scaling)

2. Constant Voltage Scaling

In full scaling, also called as full scaling, the physical dimensions of the devices are scaled down by a factor 'S' by preserving the magnitude of internal electric field in the MOSFETs. All the potentials are scaled down proportionally to attain the full scaling. While in constant voltage scaling, the physical dimensions of the MOSFETs are reduced by the factor S but the potentials are remain unchanged. The doping densities must be increased by S^2 to maintain the charge field relations. Table 1.1 shows both scaling of MOSFETs and their effects.

Table 1: Scaling of the MOSFETs and their effects

Quantity	Before scaling	After scaling	
		Constant field Scaling	Constant voltage scaling
Channel length	L	L/S	L/S
Channel width	W	W/S	W/S
Gate oxide thickness	t_{ox}	t_{ox}/S	t_{ox}/S
Power supply	V_{DD}	V_{DD}/S	V_{DD}
Threshold voltage	V_T	V_T/S	V_T
Doping Densities	N_A,N_D	S.N_A, S.N_D	S^2.N_A, S^2.N_D
Oxide capacitance	C_{ox}	S.Cox	S.C_{ox}
Drain Current	I_D	I_D/S	S.I_D
Power dissipation	P	P/S^2	S.P
Power density	P/Area	P/Area	S^3.(P/Area)

The constant voltage scaling is preferred over full scaling in various cases due to the external potential level limitations. However, the constant voltage scaling rises the current density and power density by the factor S^3 causes some serious problems such as electromigration, electrical over-stress, hot carrier degradation and oxide breakdown.

1.4 Short Channel Effects (SCEs)

It arises in the device when the effective channel length of device becomes approximately equal to thickness of depletion region at source-channel and drain-channel junctions.

1.4.1 Drain induced barrier lowering

The current conduction in the device is caused by flow of carriers from source to drain across the channel. At gate voltage less than threshold voltage i.e in the cut-off region, the potential barrier is occurred due to which flow of carriers is blocked. As the applied gate voltage increases, the potential barrier falls down. In the short channel MOSFETs, the gate and drain voltages control the potential barrier is controlled. The potential barrier decreases as the drain voltage upsurges which allows the carrier flow even if the applied gate voltage is less than the threshold voltage. This phenomena is called as drain induced barrier lowering (DIBL). The channel current is called as subthreshold current under this condition.

1.3.2 Hot carrier effects

The down scaling creates the high electric field in the channel due to which, the carriers (electrons and holes) achieved the high kinetic energies. These high energized carriers are injected into the oxide. It is called as hot carrier injection. These injected carriers are trapped into the oxide, results in increase of oxide charges and thus the threshold voltage is increased which reduce the device performance and affect the control of gate voltage on the drain current.

1.3.3 Velocity saturation

The device performance of the small geometry devices are influenced by the velocity saturation, results in decrease of the trans-conductance in the saturation region of device. At low electric field intensity, the electron drift velocity is directly proportional to the electric field. The electron drift velocity increases gradually with electric field and converges to

saturation level. Instead of pinch off, the velocity saturation restricted the drain current. This phenomena happens when device is scaling down without lowering the bias voltages.

1.5 SOI MOSFETs

In the silicon-on-insulator (SOI) MOSFET, an insulator layer called buried oxide, is introduces between the silicon layer and semiconductor substrate. It decreases the parasitic device capacitance. The silicon dioxide (SiO_2) is widely used as insulator layer.

There are many advantages of SOI MOSFETs over conventional MOSFETs as follows:

1. Lower parasitic capacitance
2. Resistance to latch up
3. Higher performance at equivalent VDD
4. Reduced temperature dependency
5. Better yield due to high density
6. Lower leakage currents

There are two types of SOI MOSFETs:

1. Partially depleted SOI (PD-SOI) MOSFETs
2. Fully depleted SOI (FD-SOI) MOSFETs

In the PD-SOI, the channel region between source and drain is partially depleted while the channel is completely depleted in case of FD-SOI. FD-SOI is preferred because of its thin size, low leakage currents and enhanced power consumption characteristics.

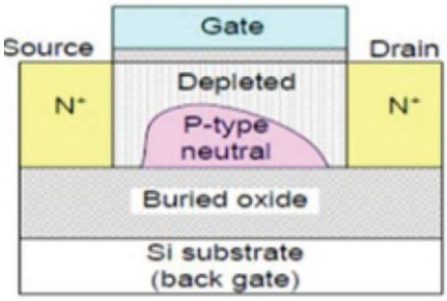

Fig. 1.5(a) Partially Depleted SOI MOSFET

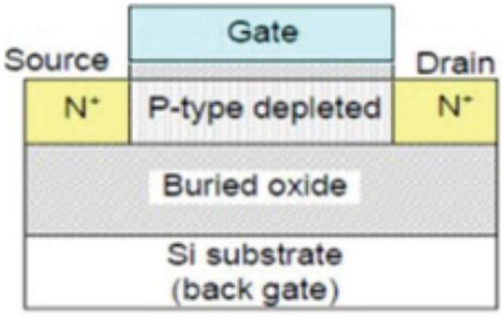

Fig. 1.5(b) Fully Depleted SOI MOSFET

However, SOI MOSFETs has admirable control on the short channel effects, but the thin source and drain regions of the device contributes high series resistance. To decrease the series resistance, the recessed-source/drain silicon-on-insulator (Re-S/D SOI) MOSFETs are established by lengthening the source and drain regions into the buried oxide (Fig. 1.6). Additionally, the Re-S/D SOI MOSFET has the coupling of bottom edge of silicon layer (back channel) to the source and drain through the buried oxide (BOX).

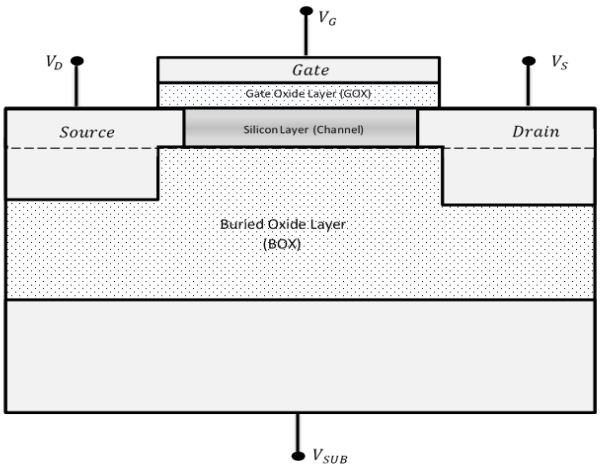

Fig. 1.6 Cross sectional view of Re-S/D SOI MOSFET

1.6 Thesis Objectives

The main objective of the thesis is to develop a novel analytic model for threshold voltage with

vertical Gaussian doping profile in the channel. The thesis covers the complete analysis of threshold modeling of Recessed source drain SOI MOSFET in which a simple approximation has made that the doping concentration in the channel in vertical direction is Gaussian while the lateral doping is uniform. Based on this approximation, the surface potential at the front and back channel is derived taking 2-D Poison's equations and appropriate boundary conditions. The threshold voltage has been expressed and analysed which is verified by the result achieved ATLAS SILVACO.

1.7 Thesis Outlines

Following this chapter introduction, the remaining part of the thesis can be summarized as follows:

Chapter-2: Literature Review

This chapter describes the literature review in which the previous work is briefed and a model of Re-S/D SOI MOSFETs is being proposed.

Chapter-3: Device Simulation Methodology

This chapter explains about the 2-D simulator software ATLAS^{TM} SILVACO which is used for verifying the result obtained from the model.

Chapter-4: Device Design

This chapter describes the variation of basic characteristics of device with physical parameters of the Re-S/d SOI MOSFETs.

Chapter-5: Mathematical Modeling

This chapter describes the mathematical modeling for surface potentials and threshold voltage

using the 2-D Poisson’s equations and boundary conditions,

Chapetr-6: Conclusion

This chapter is final section of the thesis which contains the conclusions of the complete project work.

CHAPTER 2

LITERATURE SURVEY

CHAPTER 2
LITERATURE REVIEW

2.1 Introduction

The down scaling of the MOS devices are furthermost effective approach to increase the performance of the device. Dennard [2] presented an ideal down scaling method. The potential in space charge region is high (fig 2.1), and thus, source charge carriers are appealed to the space charge region due to which the leakage current is increased. The device is scale down by a scaling factor and thus, space charge region is suppressed, causes the reduction in the leakage current. The downsizing has been very aggressive by shrinking the gate length. By taking ITRS 2008 Update [3] as reference, a roadmap has been described by H.Iwai [4] which explains a logic CMOS Technology for high performance.

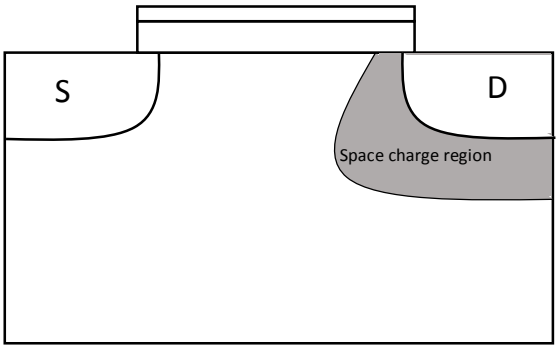

Fig 2.1 A simple MOSFET showing space charge region

However, the MOSFETs down scaling is requisite, but the short channel effects (SCEs) like high subthreshold currents, drain induced barrier lowering, hot carriers, threshold voltage roll-off etc. affect the device [5-6]. To conquer the short channel effects, a number of suggestions has been introduced this includes a retrograde doped channel [7-8], an ultra-thin source drain junction [9-10] and backside conducting layer [11]. However, for further exploration is needed for ultra-thin body MOSFETs.

The SOI technology has been advanced successively in recent years. The ultra-thin SOI

MOSFETs is introduced to investigate and analyse the short cannel effects. The SOI wafers is equipped by epitaxial layer transfer technique which is used in fabrication of SOI MOSFETs [11-15]. While scaling down, the SOI MOSFETs agonized with drawbacks that it has high source drain series resistances and low drive currents [16-19]. To overcome these problems, recessed source/drain silicon-on-insulator (Re-S/D SOI) MOSFET is proposed and implemented [20-21] which is achieved by stretching the source/drain regions into the buried-oxide (BOX).

2.2 Re-S/D SOI MOSFETs: Modeling and Simulation

The analytical models and simulations have been done for fully-depleted SOI MOSFETs by using two dimensional (2D) Poisson's equation and derived the expression of potential distribution and threshold voltage [22-28]. K. Young [22] analysed potential distribution in FD SOI MOSFETs in which the lateral electric field across the source and drain regions got affected intensely by the vertical field through the channel region due to which the short-channel effects (SCEs) is expressively pull down by shrinking the channel thickness. Since, Young has considered zero electric field at back channel and therefore, this model is independent of BOX thickness and it is also not applicable for long channel devices. The model for threshold voltage and subthreshold swing have been established with potential distribution in the channel [23-25]. K. Suzuki et al. [26] considered the 2D effects in both regions silicon and buried oxide to derive the expression for threshold voltage.

In these models, the threshold voltage has been derived by taking the assumption that the channel is uniformly doped. However, the devices is doped with ion implantation, it bear a resemblance to Gaussian distribution. The Gaussian function has maximum doping concentration N_p at straggle range R_p with standard deviation (σ_P) by which the concentration in the channel can be controlled. G. Zhang et al. [27] proposed a model for threshold voltage

of short channel single gate FD SOI MOSFETs assuming the non-uniform channel doping. The channel concentration has been taken as uniform along channel length while the concentration along the vertical direction of channel is non uniform which is Gaussian Profile. The semiconductor devices has been constantly shrinking by reducing the device dimensions which has certain technological limits and hence the replacement of device is requisite which leads to SOI technology. However, the SOI MOSFETs with ultra-thin body has admirable control of SCEs but it has a major problem that the series resistance of this device is quite high. In order to reduce this problem, the Re-S/D SOI MOSFET is used. B.Svilicic et al. [28] developed the analytic model of potential distribution in the channel and threshold voltage for Re-S/D SOI MOSFETs. Saramekala et al. [29] presented a model for threshold voltage of Re-S/D SOI MOSFETs in which dual-metal-gate (DMG) is used and described superior hot-carrier characteristic with two metal gate in series contact. Ajit Kumar et al. [30] also presented a model for the threshold voltage of short-channel Re-S/D SOI MOSFETs using the substrate induced surface potential (SISP) due to which the accuracy of model has been increased over wide range of device parameters and substrate bias. In these paper, the potential distribution at front channel and back channel are derived by taking into consideration a parabolic variation of potential perpendicular to the channel. The derivation is established by solving the two dimensional Poison's equations and using suitable boundary conditions. The analytical model result is compared and verified with the result performed using the 2-D simulator Atlas Silvaco.

2.3 Improvement Proposed

Since, the devices are doped with ion implantation, it bear a resemblance to Gaussian distribution. The analytical model for surface potential and threshold voltage of a Re-S/D SOI

MOSFETs is proposed using Gaussian distribution in the channel. The analysis of this model has a simple approximation that the doping concentration in the channel in vertical direction is Gaussian while the lateral doping is uniform. Based on this approximation, the surface potential at the front and back channel is derived taking 2D Poison's equations and appropriate boundary conditions. The threshold voltage has been expressed and analysed which is verified by the result achieved ATLAS SILVACO.

CHAPTER 3

DEVICE DESIGN

CHAPTER 3
DEVICE DESIGN

3.1 Introduction

As downsizing of the device reaches in subthreshold region, the phenomena arises called as the short channel effects [31]. The short channel effects interrupt the basic characteristics of the device as the device dimensions changes due to electrical characteristics of the materials used in the device. The basic characteristics of the devices includes threshold voltage, shubthreshold swing, on and off currents which will be varied with physical parameters of the device such as channel length, channel thickness, gate oxide thickness etc.

This chapter explains the device characteristics variation with physical device parameters of the Re-S/d SOI MOSFETs. The device is simulated in a 2-D simulator tool named ATLAS^{TM} provided by SILAVACO Inc. According to the ITRS 2011 specification for 22 nm gate length NMOS transistor, the threshold voltage (V_{th}) is 0.306V, subthreshold swing (SS) is 70mV/dec, on current (I_{on}) is 100 μA/μm and the leakage current (I_{off}) is 1582 nA/μm [4.2]. The aim of this chapter is to obtain electrical characteristics of the device detailed in ITRS 2011 specifications and thus, the physical parameter is need to be adjusted in order to maintain the specific value of electrical characteristics of the device.

3.2 Device Structure

The Re-S/D SOI MOSFETs are obtained by extending the source and drain region into the buried oxide. The fig 3.1 shows a general structure of a Re-S/D SOI MOSFET obtained from ATLAS.

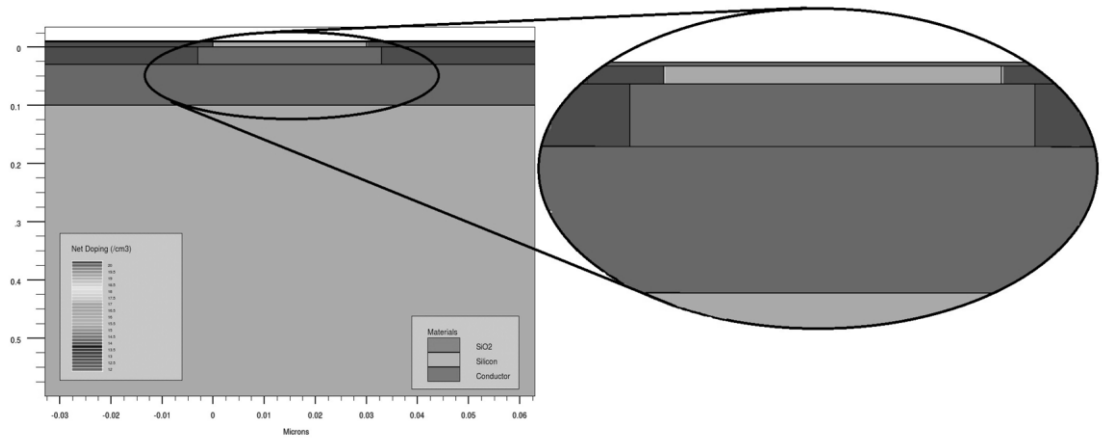

Fig 3.1 *The Re-S/D SOI MOSFET Structure in ATLAS showing the doping profile*

Table 3.1 shows the values of key parameters which is used in simulation for obtaining the electrical characteristics.

Table 3.1 Values of key parameters

Parameters	**Symbol**	**Values**
Gate length	L_G	22nm-45nm
Silicon layer (SOI) thickness	t_{Si}	2nm-20nm
Oxide thickness	t_{ox}	1nm-4nm
Thickness of the source/drain extensions into the BOX	t_{RSD}	30nm
Buried oxide thickness	t_{ox}	100nm
Source/Drain doping	N_{SD}	$1x10^{20}$ /cm^3
Channel doping	N_A	$1x10^{16}$ /cm^3
Substrate doping	N_{SUB}	$1x10^{16}$ /cm^3
Gate voltage	V_{GS}	0.2-0.4V
Drain Voltage	V_{DS}	0.2-0.4V

3.3 Simulation Results and Discussion

The electrical characteristics has been obtained with varying the channel thickness, oxide thickness and gate length. Since with downscaling the channel length the threshold voltage decreases due to short channel effects and thus in order to achieve the constant threshold voltage, the channel thickness will also have to decrease. It is clearly seen in fig 3.2 that as the device channel length is scaled down, the channel thickness will also have to reduce in order to achieve the threshold voltage 0.306V. The fig 3.2 is also describe that at fixed threshold voltage and channel length, the channel thickness is inversely proportional to oxide thickness.

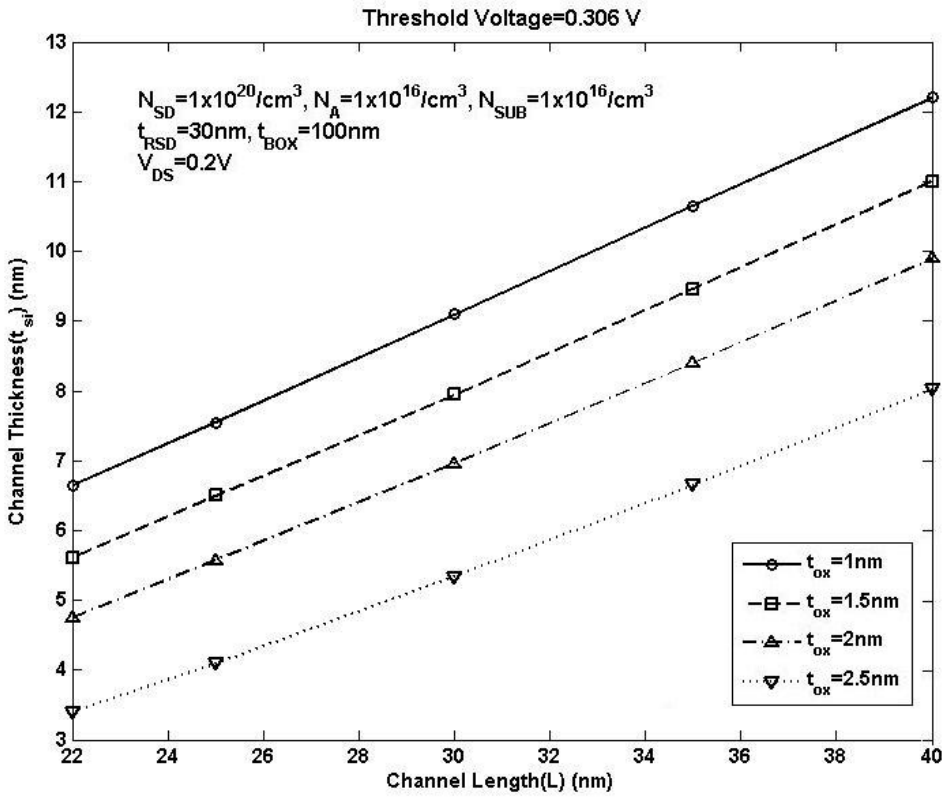

Fig.3.2 *Channel thickness vs Channel length at different oxide thickness for threshold voltage (V_{th})=0.306V*

Similarly, the physical parameters has been adjusted in order to get the optimal subthreshold

swing (SS) 70mV/dec, on current (Ion) 100uA and off current (Ioff) 1.582uA as prescribed in ITRS 2011 shown in fig 3.3, 3.4 and 3.5 respectively. In fig 3.3, the channel thickness is decreases with channel length to achieve the subthreshold swing 70mV/dec listed in ITRS.

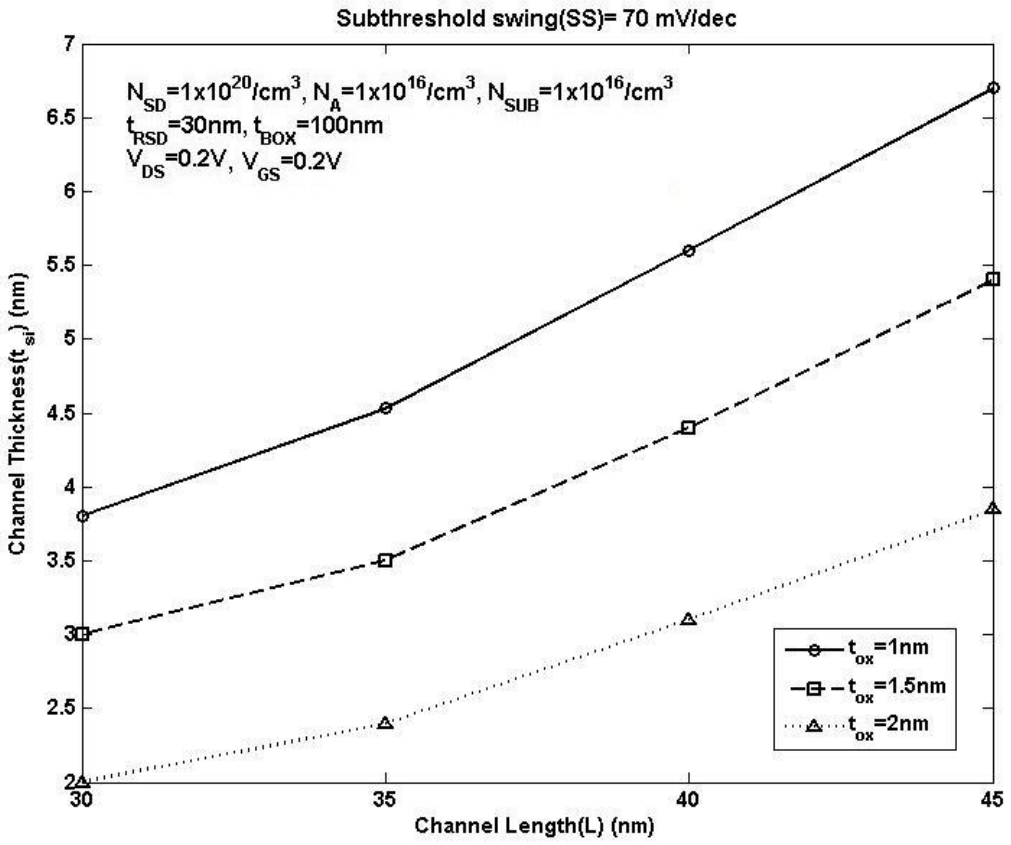

Fig.3.3 *Channel thickness vs Channel length at different oxide thickness for subthreshold swing (SS)=70mV/dec*

Fig 3.4 and 3.5 shows relation between channel thickness and gate length to achieve the optimal value of on current 100uA and leakage current 1.582uA.

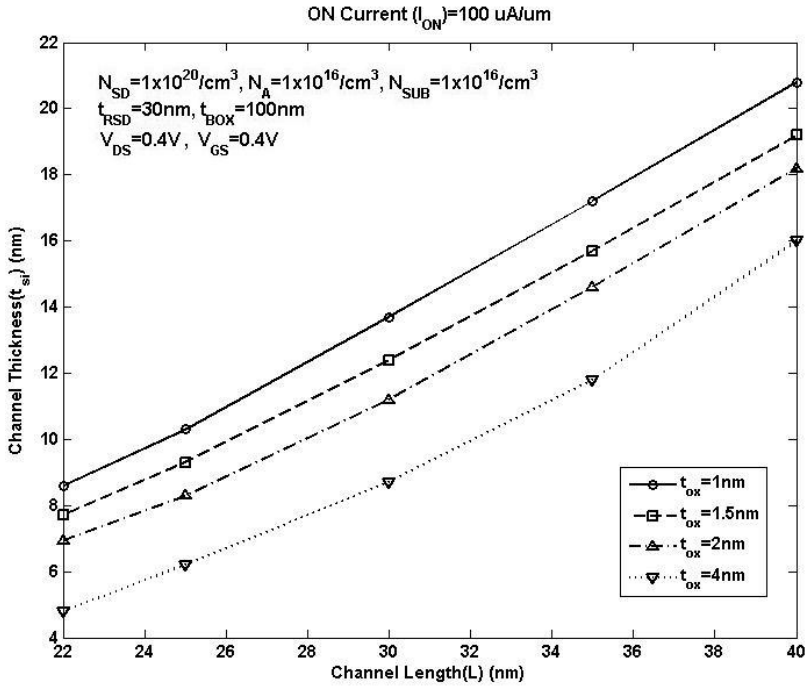

Fig.3.4 *Channel thickness vs Channel length at different oxide thickness for on current (I_{on})=100 um/um*

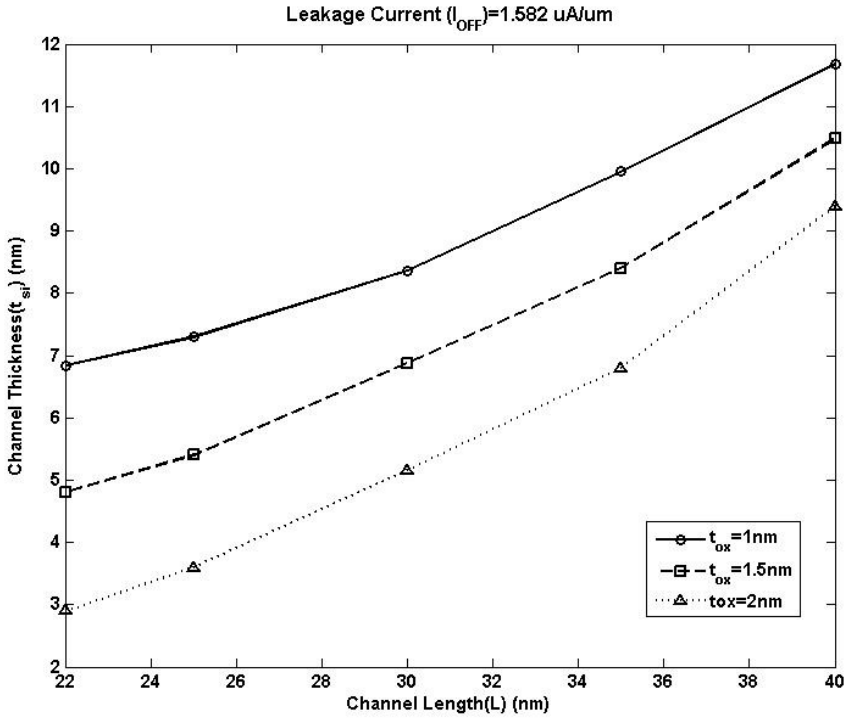

Fig.3.5 *Channel thickness vs Channel length at different oxide thickness for off current (I_{off})=1.582 uA/um*

CHAPTER 4

MATHEMATICAL MODELING OF DEVICE

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4.1 Introduction

The device models describe the device behaviour in appellation of voltage-current (V-I), voltage- capacitance (V-C) characteristics and carrier transport process which takes abode aural the device. It deals with classical, semi classical, particle and quantum transport methodologies. The device models can be divided into two categories: physical device modeling and equivalent circuit model. Physical device models describes the semiconductor equations, device geometry and doping which is used to predict the carrier transport process and terminal behaviour of the device. On the other hand, equivalent circuit models incorporate the electrical behaviour of the device. The physical device models provide detailed operation of device but it needs lengthy and complex analysis. However, closed form analytical models can be obtained based on device physics that are valid over wide range of device operation.

The analytical model comprises two-dimensional (2-D) and three dimensional (3-D) effects in the device where model equations are derived from device physics. This model is based on surface potential analysis of channel using 2-D Poisson's equation. The gate voltage is required to create the electrostatic field which causes the electrostatic potential in the channel region which is varied along the channel length. Then, the minimum surface potential and its position is calculated by solving the Poisson's equations and it is used to find the threshold voltage of the device. A number of analytical models for the threshold voltage of SOI MOSFETs has been presented. In those models, the concentration in the channel has been taken as uniform. However, the device resembles non-uniform doping in ion implantation. Here, the channel

doping profile is treated as uniform along channel length while non-uniform along vertical direction which is assumed to be a Gaussian distribution.

4.2. Theoretical Model

4.2.1 Potential Distribution

The channel of the device is doped with p-type semiconductor which is vertical Gaussian profile in nature. The channel doping concentration $N_0(y)$ can be given by

$$N_0(\mathrm{y}) = N_p \exp\left[-\frac{1}{2}\left(\frac{y-R_p}{\sigma_p}\right)^2\right] \qquad (4.1)$$

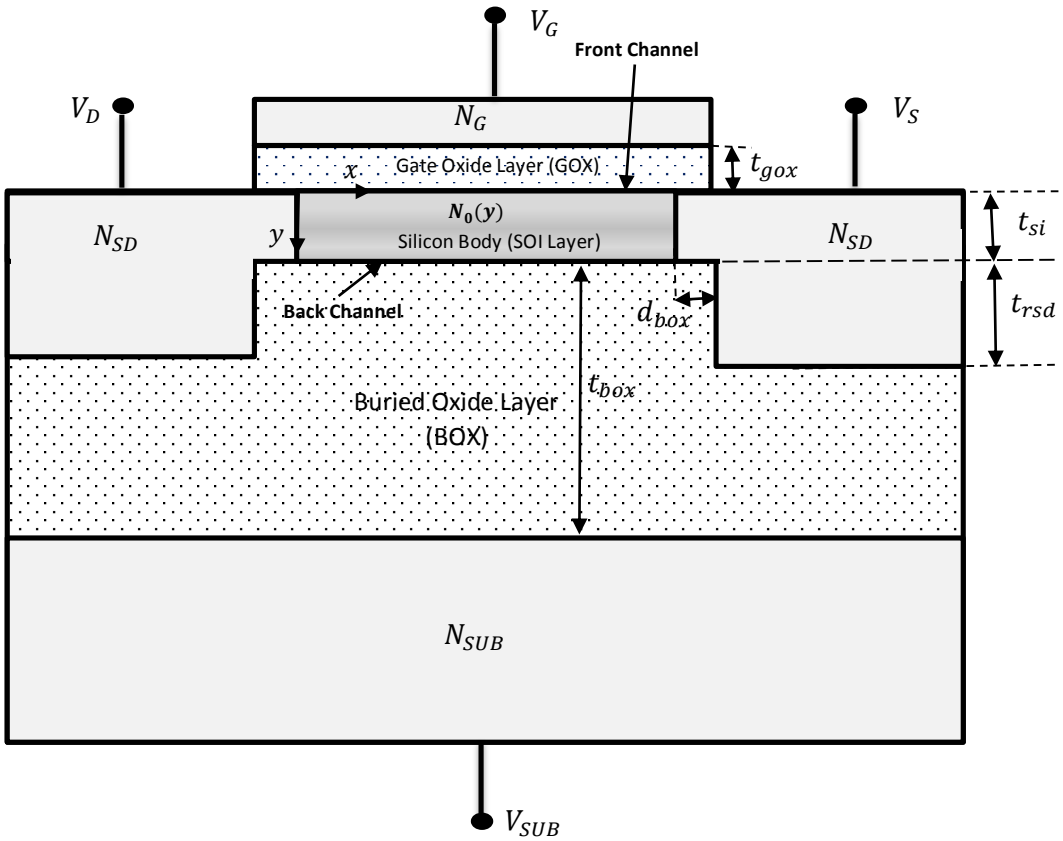

Fig. 4.1 Re-S/D SOI MOSFET structure showing device dimensions

Let us assume

$$\frac{y-R_p}{\sqrt{2}\sigma_p} = \tau \qquad (4.2)$$

From above equation,

at y=t_{Si}, $$\tau = \frac{t_{Si}-R_p}{\sqrt{2}\sigma_p} = A \qquad (4.3)$$

at y=0, $$\tau = -\frac{R_p}{\sqrt{2}\sigma_p} = B \qquad (4.4)$$

The 2D potential equation in the channel region of the recessed source/drain SOI MOSFETs which is defined by Poisson's equation, can be written as,

$$\frac{\partial^2\psi(x,y)}{\partial x^2} + \frac{\partial^2\psi(x,y)}{\partial y^2} = \frac{qN_0(y)}{k_{Si}} \qquad (0<y<t_{Si}) \qquad (4.5)$$

where

ψ(x,y)= Channel potential distribution

q = the electron charge and

k_{Si} = dielectric constant of silicon.

The equation (4.5) can be rewrite by substituting equation (4.2)

$$\frac{\partial^2\psi(x,\tau)}{\partial x^2} + \frac{1}{2\sigma_p{}^2}\frac{\partial^2\psi(x,\tau)}{\partial y^2} = \frac{qN_p}{k_{Si}}\exp(-\tau^2) \qquad (B<\tau<A) \qquad (4.6)$$

The solution of equation (4.6) can be estimated as,

$$\psi(x,\tau) = K_0(x) + K_1(x)\tau + K_2(x)\left[\tau\,\mathrm{erf}(\tau) + \frac{\exp(-\tau^2)}{\sqrt{\pi}}\right] \qquad (4.7)$$

where coefficients $K_0(x)$, $K_1(x)$ and $K_2(x)$ are functions of x only and for further calculations, it can be used as K_0, K_1 and K_2 respectively.

Poisson's Equations can be solved by using the boundary conditions as follows:

1. Potential at the front channel (x=0):

$$\psi(0, y) = \psi_f \tag{4.8}$$

2. potential at the back channel ($x=t_{Si}$):

$$\psi(t_{Si}, y) = \psi_b \tag{4.9}$$

3. Electric flux at the front channel (x=0):

$$k_{\boldsymbol{Si}}.\frac{d\psi(x,y)}{dx}|_{y=0} = k_{GOX}\frac{\psi_f-(V_G-V_{FB1})}{t_{GOX}} \tag{4.10}$$

4. Electric flux at the back channel ($x=t_{Si}$):

$$k_{si}.\frac{d\psi(x,y)}{dx}|_{y=\boldsymbol{t_{si}}} = k_{BOX}\frac{(V_D-V_{FB2})-\psi_b}{t_{RSD}} + k_{BOX}\frac{(V_S-V_{FB2})-\psi_b}{t_{RSD}} + k_{BOX}\frac{(V_{SUB}-V_{FB2})-\psi_b}{t_{RSD}} \tag{4.11}$$

5. Potential at the source-channel interface (y=0)

$$\psi(x, 0) = V_{bi} \tag{4.12}$$

6. Potential at the drain-channel interface (y=L)

$$\psi(x, L) = V_{bi}+V_{DS} \tag{4.13}$$

where k_{Si}, k_{GOX} and k_{BOX} are the dielectric constants of channel, gate oxide (GOX) and buried oxide (BOX) respectively; V_S, V_D and V_{SUB} are the source, drain and substrate voltages; V_{bi} is the built-in voltage at source/drain and channel region interface; V_{FB1}, V_{FB2} and V_{FB3} are the flat band voltages between front channel and gate, source-drain and channel and substrate and back channel respectively which can be expressed as follows:

$$V_{bi} = \left(\frac{kT}{q}\right) ln\left(\frac{N_{SD}N_0(y)}{{n_i}^2}\right) \tag{4.14}$$

$$V_{FB1} = \phi_M - \phi_{Si} \tag{4.15}$$

$$\phi_{Si} = \frac{\chi_{Si}}{q} + \frac{E_G}{2q} + \left(\frac{kT}{q}\right) ln\left(\frac{N_{SD}N_0(y=0)}{{n_i}^2}\right) \tag{4.16}$$

$$V_{FB2} = \left(\frac{kT}{q}\right) ln\left(\frac{N_{SD}N_0(y=t_{Si})}{{n_i}^2}\right) \tag{4.17}$$

$$V_{FB3} = \left(\frac{kT}{q}\right) ln\left(\frac{N_{SUB}}{n_i}\right) \tag{4.18}$$

where ϕ_M and ϕ_{Si} are the work functions of gate and silicon body, $N_0(y = 0)$ and $N_0(y = t_{Si})$ are the concentrations at front channel and back channel surfaces.

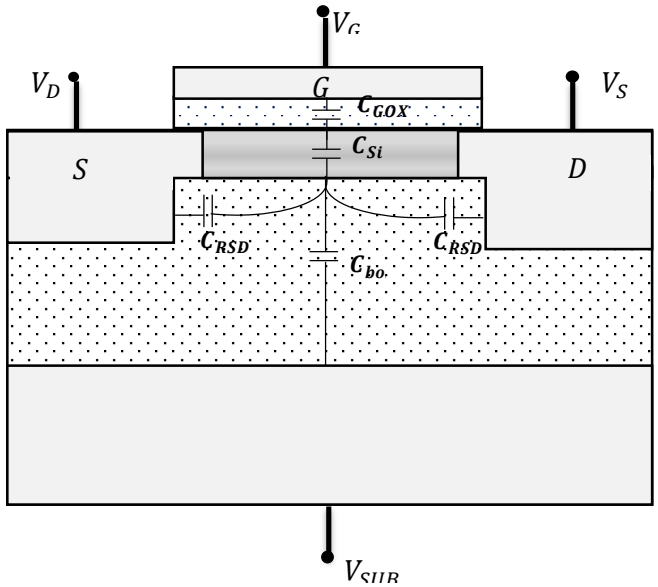

Fig. 4.2 Re-S/D SOI MOSFET structure showing the intrinsic

The fig. 4.2 shows the intrinsic capacitances in the device, which can be defined as:

1. The silicon body capacitance

$$C_{Si} = \frac{k_{Si}}{t_{Si}} \tag{4.19}$$

2. The gate oxide capacitance

$$C_{GOS} = \frac{k_{GOX}}{t_{GOX}} \tag{4.20}$$

3. The buried oxide capacitance

$$C_{BOX} = \frac{k_{BOX}}{t_{BOX}} \tag{4.21}$$

4. The recessed source-drain buried oxide

$$C_{RSD} = \frac{k_{BOX}}{t_{RSD}{}^{*}} \tag{4.22}$$

However, for the low drain voltage, the recessed source and drain will be influence by buried oxide region. Therefore, channel are connected with recessed source and drain by two identical capacitances C_{RSD} (Fig. 3.3) which can be expressed as

$$C_{RSD} = \begin{cases} \frac{k_{BOX}}{\theta} ln\left(1 + \frac{L}{2d_{BOX}}\right) & ;for\ \frac{L}{2} < t_{RSD}\ or\ t_{RSD} = 0 \\ \frac{k_{BOX}}{\theta} ln\left(1 + \frac{t_{RSD}}{2d_{BOX}}\right) & ;for\ \frac{L}{2} > t_{RSD} \end{cases} \tag{4.23}$$

Where d_{BOX} should not be zero. The angle θ the effective angle between two slanted electrode, can be calculated by

$$\theta = \frac{\pi}{2} + \frac{\pi}{2}.\operatorname{sech}\frac{t_{RSD}}{d_{BOX}} \tag{4.24}$$

The value of angle θ is varied from $\pi/2$ to π for the recessed source drain SOI MOSFTs. For the conventional SOI MOSFET, there is no overlapping of source-drain over buried oxide (BOX) i.e. $t_{RSD} = 0$ which gives the effective angle zero ($\theta = 0$). Practically, the value of θ is be minimum ($\theta = \pi/2$) if $t_{RSD} > 3d_{BOX}$ which means that the channel is coupled with source/drain regions perpendicularly.

By substituting the boundary conditions in equation (10), the coefficients K_0, K_1 and K_2 can be obtained as

$$K_0 = \psi_f - BK_1 - K_2\left\{B.\operatorname{erf}(B) + \frac{\exp(-B^2)}{\sqrt{\pi}}\right\} \tag{4.25}$$

$$K_1 = \frac{\sqrt{2}\sigma_p}{C_{Si}t_{Si}}\left\{C_{GOX}.\psi_f - C_{GOX}(V_G - V_{FB1})\right\} - \operatorname{erf}(B)K_2 \tag{4.26}$$

$$K_2 = \frac{E}{C_{Si}t_{Si}}\{C_{GOX}(V_G - V_{FB1}) + C_{RSD}(V_D - 2V_{FB2}) + C_{BOX}(V_{SUB} - V_{FB2}) - C_{GOX}.\psi_f -$$

$$(2C_{RSD} + C_{BOX}).\psi_b\} \quad (4.27)$$

where,

$$E = \frac{\sqrt{2}\sigma_p}{\exp(-A)-\exp(-B)} \quad (4.28)$$

By using equations (4.25-4.27), we can find the relation between ψ_f and ψ_b as

$$\psi_b\{t_{Si}(C_{Si} + 2C_{RSD} + C_{BOX}) + D(2C_{RSD} + C_{BOX})\} = \psi_f\{C_{Si}t_{Si} - DC_{GOX}\} +$$

$$(V_G - V_{FB1})DC_{GOX} + \{C_{RSD}(V_D - 2V_{FB2}) + C_{BOX}(V_{SUB} - V_{FB2})\}(D + t_{Si}) \quad (4.29)$$

where,

$$D = \frac{\sqrt{2}\sigma_p}{\sqrt{\pi}}.\frac{\exp(-A^2)-\exp(-B^2)}{\exp(-A)-\exp(-B)} - R_p \quad (4.30)$$

The potential is distributed over the channel in the channel which is varied in both direction, laterally and vertically. For modeling of the device for threshold voltage, the potential is needed to obtain at front surface and back surface of the channel.

In order to obtain the front channel surface potential, the expressions of the coefficients K_0, K_1 and K_2 should be in term of ψ_f only while for the back channel surface potential, the expressions of the coefficients K_0, K_1 and K_2 should be in term of ψ_b only.

Using equation (4.25-4.29), K_0, K_1 and K_2 can be written in the terms of ψ_f only as following:

$$K_0 = \psi_f - BK_1 - K_2\left\{B.\mathrm{erf}(B) + \frac{\exp(-B^2)}{\sqrt{\pi}}\right\} \quad (4.31)$$

$$K_1 = \frac{\sqrt{2}\sigma_p}{C_{Si}t_{Si}}\{C_{GOX}.\psi_f - C_{GOX}(V_G - V_{FB1})\} - \mathrm{erf}(B)K_2 \quad (4.32)$$

$$K_2 = A_{f1}(V_G - V_{FB1}) + A_{f2}\{C_{RSD}(V_D - 2V_{FB2}) + C_{BOX}(V_{SUB} - V_{FB2})\} - A_{f3}\psi_f \tag{4.33}$$

where,

$$A_{f1} = \left(\frac{E}{t_{Si}}\right)\left(\frac{C_{GOX}}{C_{Si}}\right)\left\{\frac{1+\frac{C_{Si}}{2C_{RSD}+C_{BOX}}}{1+\frac{C_{Si}}{2C_{RSD}+C_{BOX}}+\frac{D}{t_{Si}}}\right\} \tag{4.34}$$

$$A_{f2} = \left(\frac{E}{t_{Si}}\right)\left(\frac{1}{C_{Si}}\right)\left\{\frac{\frac{C_{Si}}{2C_{RSD}+C_{BOX}}}{1+\frac{C_{Si}}{2C_{RSD}+C_{BOX}}+\frac{D}{t_{Si}}}\right\} \tag{4.35}$$

$$A_{f3} = \left(\frac{E}{t_{Si}}\right)\left(\frac{C_{GOX}}{C_{Si}}\right)\left\{\frac{1+\frac{C_{Si}}{C_{GOX}}+\frac{C_{Si}}{2C_{RSD}+C_{BOX}}}{1+\frac{C_{Si}}{2C_{RSD}+C_{BOX}}+\frac{D}{t_{Si}}}\right\} \tag{4.36}$$

Similarly, using equation (4.25-4.29), K_0, K_1 and K_2 can be written in the terms of ψ_b only as following:

$$K_0 = \psi_b - AK_1 - K_2\left\{A.\,\mathrm{erf}(A) + \frac{\exp(-A^2)}{\sqrt{\pi}}\right\} \tag{4.37}$$

$$K_1 = \frac{\sqrt{2}\sigma_p}{C_{Si}t_{Si}}\{C_{GOX}(V_{SUB} - V_{FB3}) - C_{GOX}.\psi_b\} - \mathrm{erf}(A)K_2 \tag{4.38}$$

$$K_2 = A_{b1}(V_G - V_{FB1}) + A_{b2}\{C_{RSD}(V_D - 2V_{FB2}) + C_{BOX}(V_{SUB} - V_{FB2})\} - A_{b3}\psi_b \tag{4.39}$$

where,

$$A_{b1} = \left(\frac{E}{t_{Si}}\right)\left(\frac{C_{GOX}}{C_{Si}}\right)\left\{\frac{\frac{C_{Si}}{C_{GOX}}}{\frac{C_{Si}}{C_{GOX}}-\frac{D}{t_{Si}}}\right\} \tag{4.40}$$

$$A_{b2} = \left(\frac{E}{t_{Si}}\right)\left(\frac{C_{GOX}}{C_{Si}}\right)\left\{\frac{\frac{1}{C_{GOX}}\left(1+\frac{C_{Si}}{C_{GOX}}\right)}{\frac{C_{Si}}{C_{GOX}}-\frac{D}{t_{Si}}}\right\} \tag{4.41}$$

$$A_{b3} = \left(\frac{E}{t_{Si}}\right)\left(\frac{C_{GOX}}{C_{Si}}\right)\left\{\frac{\frac{C_{Si}}{C_{GOX}}+\frac{1}{C_{GOX}}\left(1+\frac{C_{Si}}{C_{GOX}}\right)(2C_{RSD}+C_{BOX})}{\frac{C_{Si}}{C_{GOX}}-\frac{D}{t_{Si}}}\right\} \quad (4.42)$$

Now, using the expressions of coefficients K_0, K_1 and K_2 and by differentiating the equation (4.7) at x=0 and at x=t_{Si} , we get,

$$\frac{\partial^2\psi_f}{\partial y^2} - \alpha_f\psi_f = \beta_f \quad (4.43)$$

$$\frac{\partial^2\psi_b}{\partial y^2} - \alpha_b\psi_b = \beta_b \quad (4.44)$$

where,

$$\alpha_f = \frac{\exp(-B^2)}{\sqrt{\pi}{\sigma_p}^2} A_{f3} \quad (4.45)$$

$$\beta_f = \frac{qN_p}{k_{Si}}\exp(-B^2) - \frac{\exp(-B^2)}{\sqrt{\pi}{\sigma_p}^2}\Big\{A_{f1}(V_G - V_{FB1}) + A_{f2}\{C_{RSD}(V_D - 2V_{FB2}) + C_{BOX}(V_{SUB} - V_{FB2})\}\Big\} \quad (4.46)$$

$$\alpha_b = \frac{\exp(-A^2)}{\sqrt{\pi}{\sigma_p}^2} A_{b3} \quad (4.47)$$

$$\beta_b = \frac{qN_p}{k_{Si}}\exp(-A^2) - \frac{\exp(-A^2)}{\sqrt{\pi}{\sigma_p}^2}\Big\{A_{b1}(V_G - V_{FB1}) + A_{b2}\{C_{RSD}(V_D - 2V_{FB2}) + C_{BOX}(V_{SUB} - V_{FB2})\}\Big\} \quad (4.48)$$

The equations (4.43) and (4.44) is the second order non-homogenous differential equations for front channel surface and back channel surface respectively.

By solving the equations (4.43) and (4.44) with boundary conditions, the expression of front and back channel surface potential can be obtain as

$$\psi_f = A_f e^{\sqrt{\alpha_f}x} + B_f e^{-\sqrt{\alpha_f}x} - \frac{\beta_f}{\alpha_f} \quad (4.49)$$

$$\psi_b = A_b e^{\sqrt{\alpha_b}x} + B_b e^{-\sqrt{\alpha_b}x} - \frac{\beta_b}{\alpha_b} \tag{4.50}$$

where,

$$A_f = \frac{\beta_f\left(e^{\sqrt{\alpha_f}L}-1\right)+\alpha_f\left\{V_{bi}\left(e^{\sqrt{\alpha_f}L}-1\right)+V_{DS}.e^{\sqrt{\alpha_f}L}\right\}}{\alpha_f\left(e^{2\sqrt{\alpha_f}L}-1\right)} \tag{4.51}$$

$$B_f = \frac{e^{\sqrt{\alpha_f}L}\left[\beta_f\left(e^{\sqrt{\alpha_f}L}-1\right)+\alpha_f\left\{V_{bi}\left(e^{\sqrt{\alpha_f}L}-1\right)-V_{DS}\right\}\right]}{\alpha_f\left(e^{2\sqrt{\alpha_f}L}-1\right)} \tag{4.52}$$

$$A_b = \frac{\beta_b\left(e^{\sqrt{\alpha_b}L}-1\right)+\alpha_b\left\{V_{bi}\left(e^{\sqrt{\alpha_b}L}-1\right)+V_{DS}.e^{\sqrt{\alpha_b}L}\right\}}{\alpha_b\left(e^{2\sqrt{\alpha_b}L}-1\right)} \tag{4.53}$$

$$B_b = \frac{e^{\sqrt{\alpha_b}L}\left[\beta_b\left(e^{\sqrt{\alpha_b}L}-1\right)+\alpha_b\left\{V_{bi}\left(e^{\sqrt{\alpha_b}L}-1\right)-V_{DS}\right\}\right]}{\alpha_b\left(e^{2\sqrt{\alpha_b}L}-1\right)} \tag{4.54}$$

The equations (4.49) and (4.50) show the variation of the front and back surface potentials which varies along the channel length. For the threshold voltage calculation, the minimum surface potential in the channel is required to determine. Hence, we have to differentiate the equations (4.49) and (4.50) and equate it to zero which gives the position of minimum front and back channel surface potential respectively as

$$x_{f,min} = \frac{1}{\sqrt{\alpha_f}} ln\left(\frac{B_f}{A_f}\right) \tag{4.55}$$

$$x_{b,min} = \frac{1}{\sqrt{\alpha_b}} ln\left(\frac{B_b}{A_b}\right) \tag{4.56}$$

Equations (4.55) and (4.56) position of minimum potential at front and back. It varied with the drain voltage. As the drain voltage increases, it shifted towards the source end. By substituting

these values in the equations (4.49) and (4.50), the minimum front and back channel surface potentials is obtained which is given by,

$$\psi_{f,min} = \psi_f\big|_{x=x_{f,min}} \tag{4.57}$$

$$\psi_{b,min} = \psi_b|_{x=x_{b,min}} \tag{4.58}$$

4.2.2 Threshold Voltage

The minimum gate voltage required to generate the conduction current between source and drain is called as threshold voltage. In other words, the threshold voltage is defined as the applied gate voltage for which surface potential becomes minimum and equals to the twice of Fermi voltage of the channel.

For threshold voltage modeling, we can take its definition according to which it is the gate voltage at which the minimum surface potential equals to the value of $2\phi_f$, where ϕ_f is the Fermi voltage which can be expressed as

$$\phi_f = \frac{kT}{q}\, ln\left(\frac{N_0}{n_i}\right) \tag{4.59}$$

In the Re-S/D SOI MOSFETs, the larger among the front channel surface potential and back channel surface potential is considered as the threshold voltage. Hence, the threshold voltage is given by

$$V_{th} = V_G|_{max[\varphi_{f,min},\varphi_{min,b}]=2\phi_f} \tag{4.60}$$

The equation (4.60) is the expression of threshold voltage which gives two expression of threshold voltage, V_{thf} and V_{thb} which can be obtained by equating the minimum front and back channel surface potential to $2\phi_f$.

Now in order to obtain the threshold voltage V_{thf}, we have to rewrite the expressions of A_f, B_f, β_f in terms of gate voltage $V_G{}'(= V_G - V_{FB1})$ as

$$A_f = u_{1f}.V_G{}' + v_{1f} \tag{4.61}$$

$$B_f = u_{2f}.V_G{}' + v_{2f} \tag{4.62}$$

$$\beta_f = m_f.V_G{}' + n_f \tag{4.63}$$

Now equating the minimum front channel surface potential to $2\phi_f$ from equations (4.61-4.63) and replacing $V_G{}'$ with $V_{thf}{}'$ where $V_{thf}{}' = V_{thf} - V_{FB1}$, we get

$$a_f V_{thf}{}'^2 + b_f V_{thf}{}' + c_f = 0 \tag{4.64}$$

where,

$$a_f = u_{1f}u_{2f} - \left(\frac{m_f}{2\alpha_f}\right)^2 \tag{4.65}$$

$$b_f = u_{1f}v_{2f} + v_{1f}u_{2f} - \frac{m_f.n_f}{2\alpha_f{}^2} - \frac{m_f}{\alpha_f}\phi_f \tag{4.66}$$

$$c_f = v_1 v_2 - \phi_f \mathrm{b}^2 - \left(\frac{n_f}{2\alpha_f}\right)^2 - \frac{n_f}{\alpha_f}\phi_f \tag{4.67}$$

Now in order to obtain the threshold voltage V_{thb}, we have to rewrite the expressions of A_b, B_b, β_b in terms of gate voltage $V_G{}'(= V_G - V_{FB1})$ as

$$A_b = u_{1b}.V_G{}' + v_{1b} \tag{4.68}$$

$$B_b = u_{2b}.V_G{}' + v_{2b} \tag{4.69}$$

$$\beta_b = m_b.V_G{}' + n_b \tag{4.70}$$

Now, equating the minimum back channel surface potential to $2\phi_f$ rom equations (4.61-4.63) and replacing $V_G{}'$ with $V_{thb}{}'$ where $V_{thb}{}' = V_{thb} - V_{FB3}$, we get

$$a_b {V_{thb}}'^2 + b_b V_{thb}{}' + c_b = 0 \tag{4.71}$$

where,

$$a_b = u_{1b}u_{2b} - \left(\frac{m_b}{2\alpha_b}\right)^2 \tag{4.72}$$

$$b_b = u_{1b}v_{2b} + v_{1b}u_{2b} - \frac{m_b.n_b}{2{\alpha_b}^2} - \frac{m_b}{\alpha_f}\phi_f \tag{4.73}$$

$$c_b = v_1 v_2 - {\phi_f}^2 - \left(\frac{n_b}{2\alpha_b}\right)^2 - \frac{.n_b}{\alpha_b}\phi_f \tag{4.74}$$

By solving the quadratic equations (4.64) and (4.71), the threshold voltage can be expressed as

$$V_{thf} = \frac{-b_f \pm \sqrt{{b_f}^2 - 4a_f c_f}}{2a_f} + V_{FB1} \tag{4.75}$$

$$V_{thb} = \frac{-b_b \pm \sqrt{{b_b}^2 - 4a_b c_b}}{2a_b} + V_{FB3} \tag{4.76}$$

Since, V_{thf} and V_{thb} are the threshold voltage corresponding to front channel and back channel surface. It means that the device is tuned on when adequate amount of current flows either on front channel or back channel. The conduction starts at front channel before back channel if the front channel surface potential is larger while conduction starts at back channel before front channel if the back channel surface potential is larger which ensure the threshold voltage of the device.

Hence, final threshold voltage can be determined by

$$V_{th} = \begin{cases} V_{thf} & ; \psi_{f,min} > \psi_{b,min} \\ V_{thb} & ; \psi_{f,min} < \psi_{b,min} \end{cases} \tag{4.77}$$

4.3 Results and Discussions

The surface potentials at front and back channel and threshold voltage has been expressed in equations (4.49), (4.50) and (4.77) respectively. Now the surface potential and threshold voltage at front and back channel are extracted from the device simulator ATLAS.

In ATLAS, the threshold voltage can be extracted form I_D-V_G graph. It is determined as the gate voltage where the drain current I_{Dth} reached at the specific value, which is given by

$$I_{Dth}=1x10^{-7}.(W_L/L_G)$$

Where, W_L is the channel width, and L_G is the gate length. While simulation of device in ATLAS, the channel width is taken as 1µm.

The potential distribution in the device can be seen in fig. 4.3 with L=50nm at drain voltage 0.2V. The minimum surface potential at both front and back channel is shift towards source from middle of channel. The minimum surface potential will be at centre of channel if drain bias is zero. The potential distribution at front and back channel surface along the channel length is shown in the fig. 4.3.

Although the minimum potential drop for back channel is more as compared to minimum potential for front channel, the back channel surface potential dominates the threshold voltage. Since, a p -type base silicon concentration is used, and hence the surface potential at front channel (V_{thf}) is smaller than the surface potential at back channel (V_{thb}). When low-doped substrates is used, then the back channel potential dominates the threshold voltage.

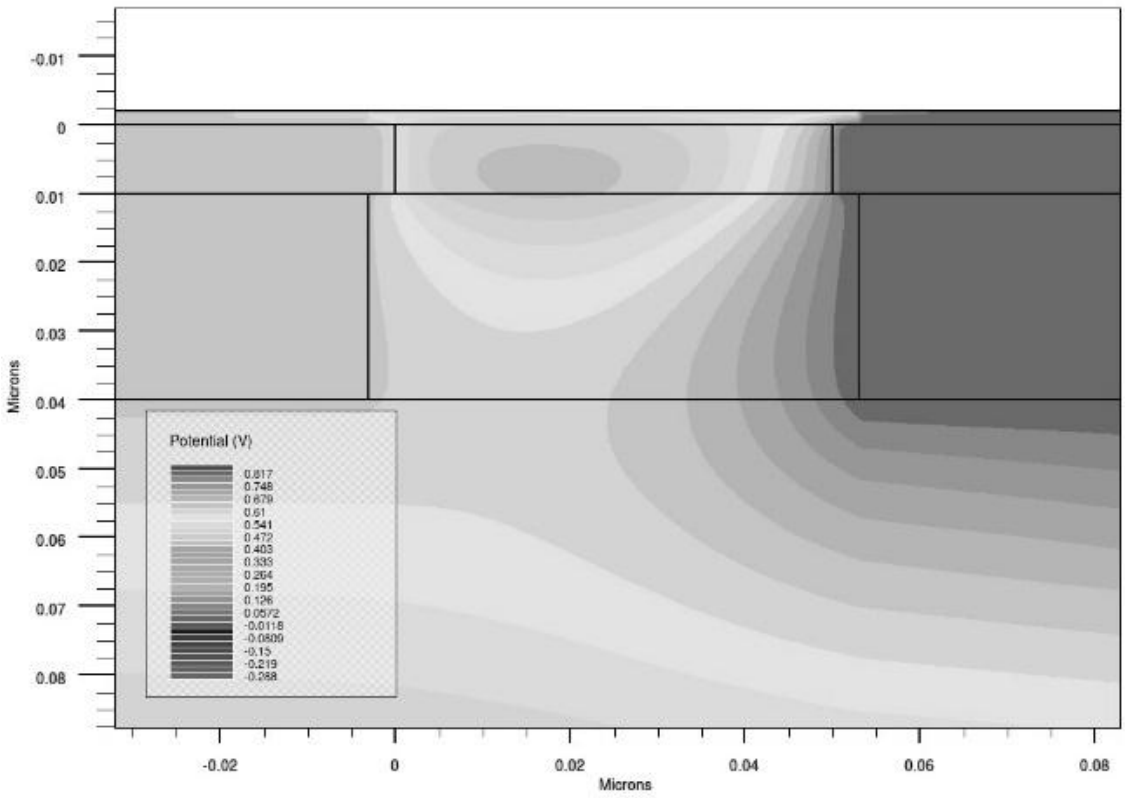

Fig. 4.3 The distribution of potential in the device with L=50 nm

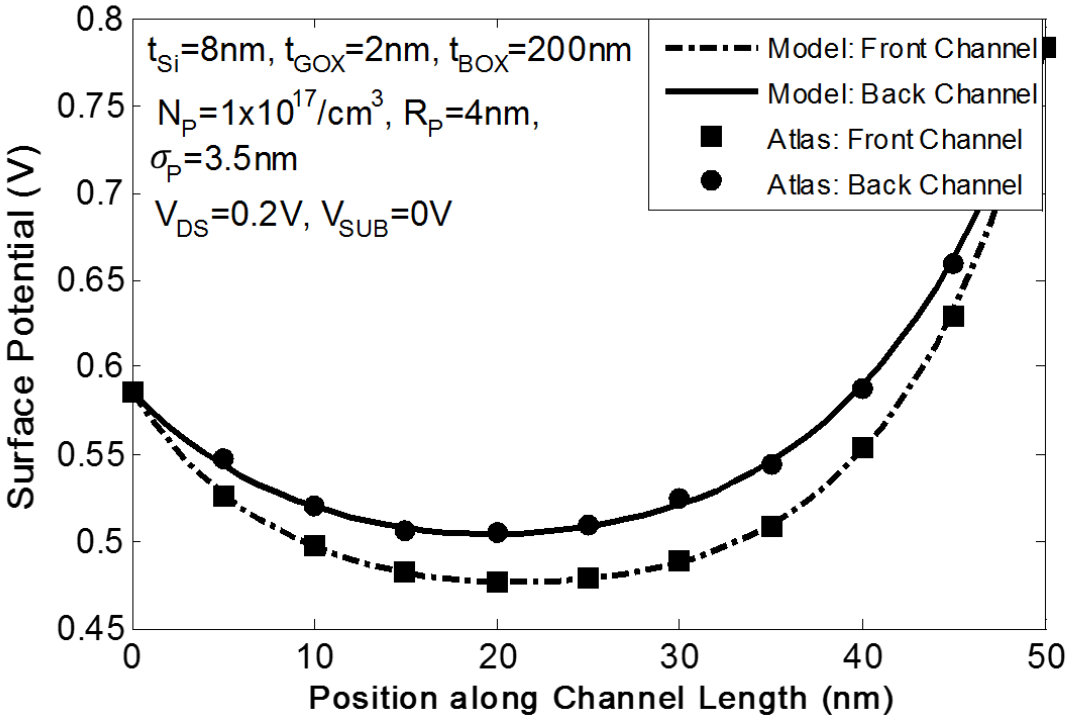

Fig. 4.4 Front and back channel potential distribution along the channel with L=50 nm.

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The threshold voltage in equation (4.77) has been obtained from minimum surface potential formulated in equation (4.57) and (4.58). The analytic model result of threshold voltage is verified from result extracted from device simulator ATLAS. Since, the channel is doped with the Gaussian profile, the total doping concentration in the channel is dependent at on Gaussian parameters peak concentrations (Np), projected deviation (σ_P) and projected range (R_P). Fig. 4.5-4.7 shows the dependency of threshold voltage (Vth) on different peak concentrations (Np), projected deviation (σ_P) and projected range (R_P) of the Gaussian distribution of doping profile.

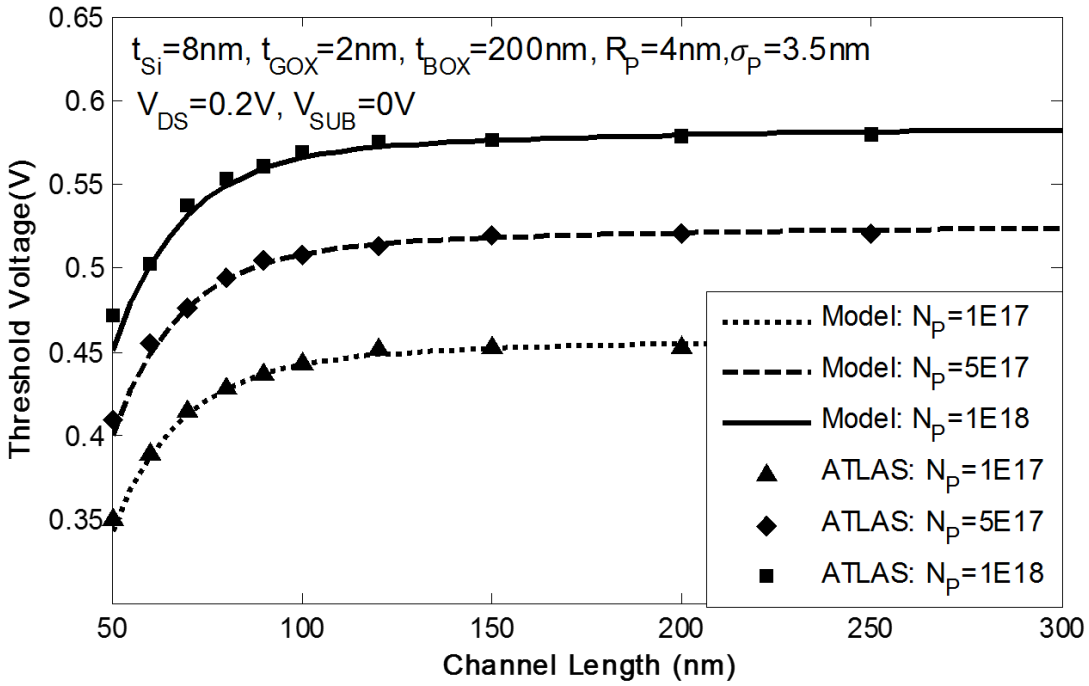

Fig 4.5 Variation of the threshold voltage with gate length with Gaussian profile for different peak concentration

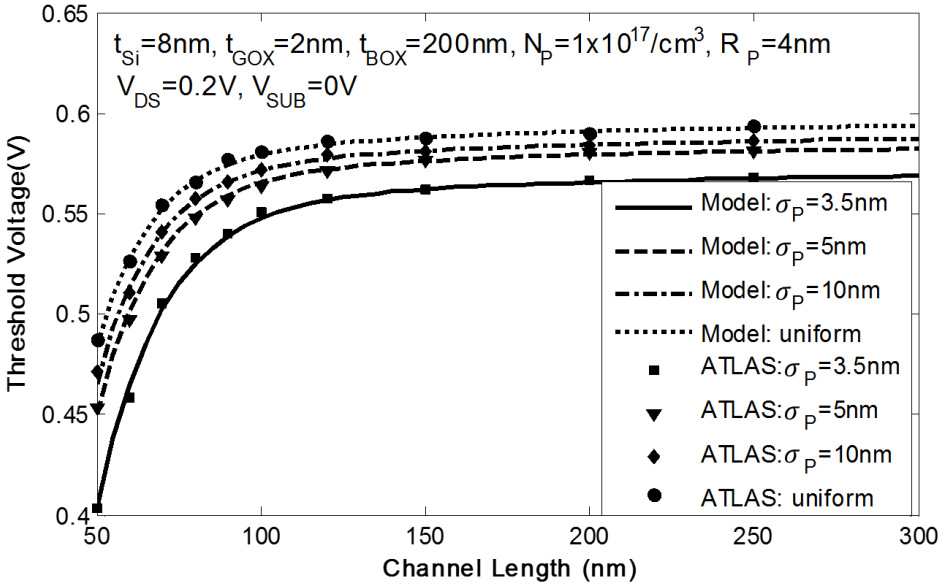

Fig 4.6 Variation of the threshold voltage with gate length with Gaussian profile for different project deviation

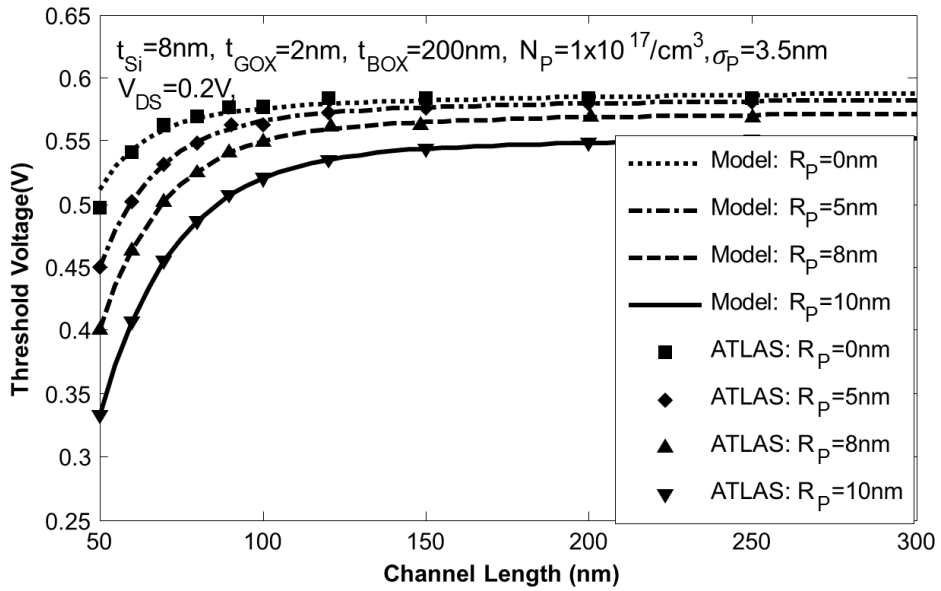

Fig 4.7 Variation of the threshold voltage with gate length with Gaussian profile for different project range

For longer channel length, the threshold voltage as almost constant but as the channel length decreases, the short-channel effects are introduced due to the reduction of channel length

causes the smaller threshold voltage. In fig 4.4, as the peak concentration increases, the total concentration in the channel increases, and thus the threshold voltage is also increased. The same tendency can been be seen for R_P and σ_P in fig 4.5 and 4.6. As the σ_P increases, Gaussian doping distribution approaches to uniform doping, and total doping concentration in the channel region increases due to which the threshold voltage is upsurge but the short channel immunity is relatively unaffected. The threshold voltage is also dependent on physical parameters of device. Fig. (4.8-11) show the variation of threshold voltage with physical parameters of the device such as channel thickness (t_{Si}), GOX thickness (t_{GOX}), BOX thickness (t_{BOX}) and source/drain extension. In case of thinner channel (fig. 4.8), the back channel surface potential is affected more than front channel surface potential and thus, the short channel immunity advances and threshold voltage increases.

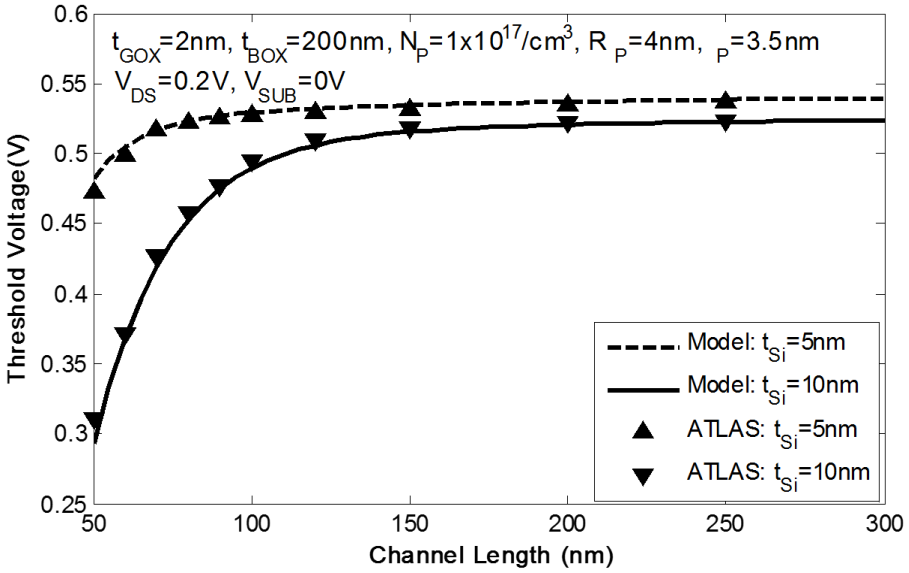

Fig 4.8 Variation of the threshold voltage with gate length with Gaussian profile for different channel thickness

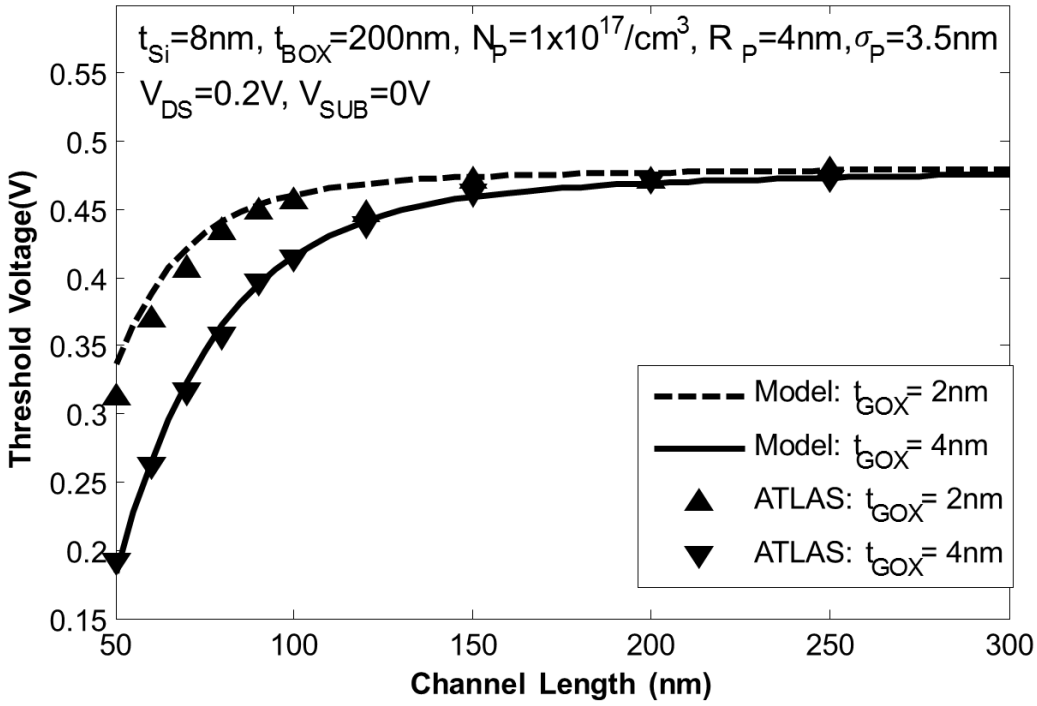

Fig 4.9 Variation of the threshold voltage with gate length with Gaussian profile for different gate oxide thickness

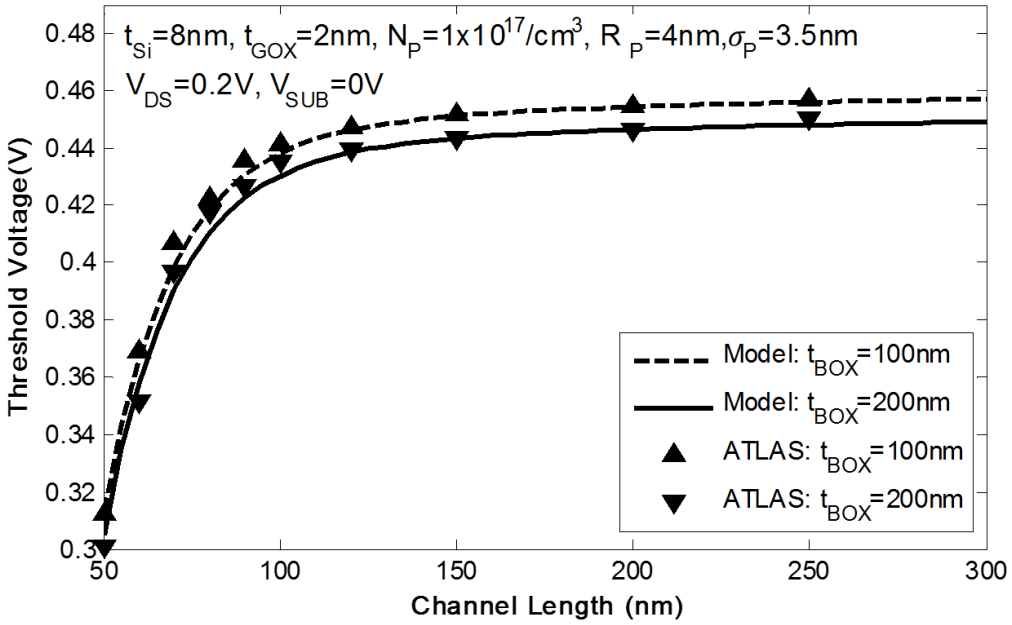

Fig 4.10 Variation of the threshold voltage with gate length with Gaussian profile for different buried oxide thickness

With reduction of GOX thickness, C_{GOX} is enlarged and threshold voltage increases and thus short channel immunity improves. The threshold voltage is also increased with reduction of BOX thickness (fig. 4.10) but the short channel immunity is marginally reduced because the applied gate voltage is comparatively expended more over the BOX.

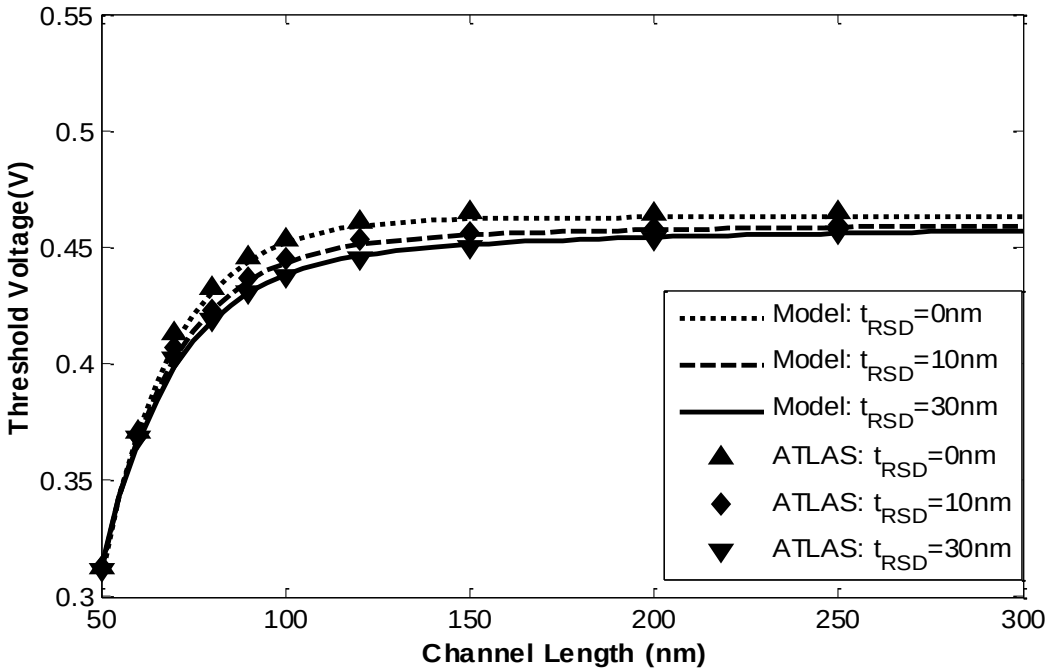

Fig 4.11 Variation of the threshold voltage with gate length with Gaussian profile for different depth of recessed region

The threshold voltage is little bit influenced by the thickness of recessed source/drain t_{RSD} which allowing extensive choice in the design of Re/S/D SOI MOSFET with respect to threshold voltage. The device will act as conventional SOI MOSFET at t_{RSD}=0. The capacitance C_{BOX} is calculated from equation 4.23 with $\theta=\pi$. Fig. 4.11 shows the threshold voltage variation with gate length at different thicknesses of recessed region. Foe all the cases, this model is compared with result simulated in ATLAS which shows a very good agreement.

CHAPTER 6

CONCLUSION

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CONCLUSION

In the downscaling, the basic electrical characteristics varied due to the short channel effects. The SCEs degrades the performance of the device. The physical parameters has been designed in order to achieve the electrical characteristics like threshold voltage, subthreshold swing, on and off currents as detailed in ITRS 2011 specifications.

The threshold voltage for the FD Re-SOI MOSFETs has been successfully modelled. The potential distribution is obtained using 2D Poison's equations and proper boundary conditions by taking vertical Gaussian doping in the channel which is used to find the expression of threshold voltage. Then, this analytic model is compared by results simulated in the 2D simulator ATLAS SILVACO with different channel length (t_{Si}), gate oxide (t_{GOX}), buried oxide (t_{BOX}) and recessed source/drain thickness (t_{RSD}). The model result has been matched with simulation result.

APENDIX

APENDIX

A.1 Gaussian Distribution

It is named after the mathematician Carl Friedrich Gauss. It is also called as "bell shaped curve". It is a continuous distribution.

Mathematically, the Gaussian function is defined as,

$$N_0(\mathrm{y}) = N_p \exp\left[-\frac{1}{2}\left(\frac{y-R_p}{\sigma_p}\right)^2\right]$$

where,

$N_0(\mathrm{y})$ = The channel doping concentration

N_p = Maximum doping (Peak concentration) in the channel

R_p = Position of peak concentration / mean of distribution

${\sigma_p}^2$ = Variance of distribution

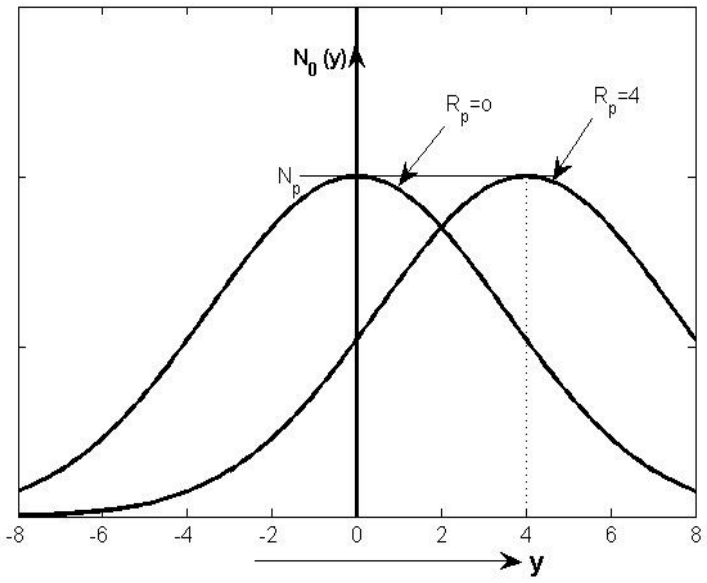

Fig. A.1 Guassian distribution

By introducing a variable ‘c’ as

$$c = \sqrt{2\sigma_p{}^2}$$

Using above variable, the Gaussian function can be expressed as

$$N_0(\mathrm{y}) = N_p \exp\left[-\left(\frac{y-R_p}{c}\right)^2\right]$$

Syntax for Atlas:

doping gaussian characteristic=*c* peak=R_p conc=N_p *type of semiconductor* region=*n* / direction=*y*

where,

type of semiconductor will be **n.type** for n-type and **p.type** for p-type semiconductor

region defines the region number (n) and

direction may be either **x** or **y**

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